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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Atty. Docket
COENEN	NL 010013
Serial: 10/042,464	Group Art Unit: 2116
Filed: 01/08/2002	Examiner: CHEN, TSE W

POWER MANAGEMENT FOR DIGITAL PROCESSING SYSTEM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Charge Authorization and Extension of Time Statement

The Commissioner is hereby requested and authorized pursuant to 37 CFR §1.136(a)(3), to treat any concurrent reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. Please charge any additional fees which may now be required in this application, including extension of time fees, to Deposit Account No. 50-4019.

Respectfully submitted,

John Rehberg, Reg. 29,207

Dated: 7-30-07

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	COENEN
Application No.	:	10/042,464
Filed	:	01/08/2002
For	:	POWER MANAGEMENT FOR DIGITAL PROCESSING APPARATUS

APPEAL BRIEF

On Appeal from Group Art Unit 2116

Date: 07/30/2007

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

Certificate of Fax/Mailing Under 37 CFR 1.8

I hereby certify that this correspondence is being faxed to (571)273-8300 or deposited with the United States Postal Service as first class mail in an envelope addressed to the COMMISSIONER FOR PATENTS, Mail Stop Appeal, P.O. BOX 1450 ALEXANDRIA, VA 22313 on date below.

Michael Ure
(Name)

M Ure 7/30/07
(Signature and Date)

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NONE

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-10 are pending, all of which stand finally rejected and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a clocking arrangement for an integrated circuit. To conserve power, it is common for an integrated circuit or portions thereof to be placed in a low power condition during periods of disuse. However, when power is re-supplied

to the integrated circuit or portions thereof, a current surge is experienced. This current surge may result in supply line bounce. Dealing with the current surge and suppressing supply line bounce requires various measures that entail expense and complexity and that may reduce performance. The present invention solves this problem by gradually (rather than abruptly) increasing the supply current to a digital processing apparatus, in the following manner. A plurality of sub-clocking signals are generated from a master clock signal. The sub-clocking signals change from a power-up rest condition to a continuously free running condition one at a time following an initial switch-on of the digital processing apparatus.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A method of power management in a digital processing apparatus, the method comprising:		
receiving a free-running master clock signal; and	Fig. 1, CLK; Fig. 2, CLK.	Page 3, line 20 to page 5, line 19
generating a plurality of sub-clocking signals from said master clock signal,	Fig. 1, CLK0-CLK3; Fig. 2, CLK0-CLK3.	Page 3, line 20 to page 5, line 19
wherein said plurality of sub-clocking signals change from a power-up rest condition to a continuously free running condition one at a time, following an initial switch-on of said digital processing apparatus.	Fig. 1: a, b, c, d; Fig. 2: a, b, c, d.	Page 3, line 20 to page 5, line 19

The following analysis of independent claim 2 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
2. A device for power management for a digital processing apparatus, the method comprising:		
means (10,20) for receiving a continuously free-running master clock signal; and	Fig. 1: 10, 20	Page 3, line 20 to page 5, line 19
means (10, 20) for generating a plurality of sub-clocking signals from said master clock signal,	Fig. 1: 10, 20	Page 3, line 20 to page 5, line 19
wherein said plurality of sub-clocking signals change from a power-up rest condition to a continuously free running condition one at a time, following an initial switch-on of said digital processing apparatus (30).	Fig. 1: a, b, c, d; Fig. 2: a, b, c, d.	Page 3, line 20 to page 5, line 19

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 103(a), claims 1-10 are anticipated by Smentek.

VII. ARGUMENT

I. Rejection of Claims 1-10 as Anticipated by Smentek

Smentek relates to an arrangement for reducing power consumption in a digital processing apparatus ("digital processor"). This is accomplished by eliminating continuously free running clocks to various portions of the digital processor and instead providing clock pulses on an "as needed basis." To reduce the "step load" encountered in such a system, a mechanism is provided to ensure that some minimum desired "base" power consumption is maintained. The step between base level power consumption and full power consumption is thereby reduced.

The construction of the Smentek device can be well-appreciated from the cover figure (Figure 3) thereof. A pipelined data processing circuit having multiple pipeline stages (functional blocks FB1-FB1) receives data in and processes the data in to produce data out. Latches are provided between each of the pipeline stages. The operation of the respective stages is triggered by respective firing signals FIRE1, FIRE2, etc., produced by coincidence of a respective enable signal (EN1-EN8) and a clock signal. A two-phase clock is provided having phases CLK and NCLK. The stages are alternately clock on different clock phases (stage 1, NCLK; stage 2, CLK, etc). Note the timing diagram shown in Figure 2 of Smentek. Figure 2 of Smentek may be contrasted with Figure 2 of the present specification, showing continuously free running sub-clock signals CLK1-CLK3 having staggered start times.

Operation of the pipeline of Smentek is started by either a START signal or a DUMMY START signal. Operation triggered by the START signal produces useful data. Operation triggered by the DUMMY START signal produces data that is ignored.

Dummy start generation logic 374 compares the activity level of the pipeline with the desired activity level stored in register 384 and generates DUMMY START signals accordingly.

In this construction, the clock signals EN1-EN8 are generated from the two-phase clock CLK, NCLK on an as-needed basis as seen in Fig. 2. Only the two-phase clock CLK, NCLK is continuously free running. Hence, there are *no continuously free running sub-clock signals* generated from a master clock as claimed.

The examiner apparently takes the position that because DUMMY START signals are generated in Smentek to activate the pipeline more frequently than required by data processing operations themselves, the triggering pulses of Smentek are therefore somehow "continuously free running." This is not the case. Even if the apparatus of Smentek were configured such that the pipeline operated at maximum throughput, whether with real operations, dummy operations, or some combination thereof, the trigger pulses of Smentek would not be continuously free running because of the nature of the pipeline apparatus. In a pipeline of N stages such as that of Smentek, each stage is clocked at a rate that is 1/N the rate of the master clock. The clocks of the respective stages are therefore, necessarily, gated in a "one-shot" manner by the state machine 315 of Smentek.

It may therefore be seen that Smentek does not anticipate the invention of claim 1 or the invention of claim 2.

With regard to dependent claims 3-10, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference.

Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claim.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: 7/30/07

By: Michael Ure
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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A method of power management in a digital processing apparatus, the method comprising: receiving a free-running master clock signal; and generating a plurality of sub-clocking signals from said master clock signal, wherein said plurality of sub-clocking signals change from a power-up rest condition to a continuously free running condition one at a time, following an initial switch-on of said digital processing apparatus (30).

2. A device for power management for a digital processing apparatus, the device comprising: means (10, 20) for receiving a continuously free running master clock signal; and means (10, 20) for generating a plurality of sub-clocking signals from said master clock signal, wherein said plurality of sub-clocking signals change from a power-up rest condition to a continuously free running condition one at a time, following an initial switch-on of said digital processing apparatus (30).

3. A device according to claim 2, wherein each sub-clocking signal is used to clock a separate data processing part (30_0-30_3) of said apparatus (30).

4. A device according to claim 3, wherein each data processing part (30_0-30_3) comprises circuitry for processing a particular serial data bit or bits of a data word.

5. A device according to claim 4, wherein said digital signal processing apparatus has a particular maximum data width and wherein said plurality of sub-clocking signals corresponds to said maximum data width.

6. A device according to claim 2, wherein during a switch-off phase of said digital processing apparatus, said plurality of sub-clocking signals change from a continuously free running condition to a rest condition one at a time.

7. A device according to claim 2, wherein said means for receiving a master clocking

signal and generating a plurality of sub-clocking signals comprise: a shift register (10) for providing a plurality of enabling signals, said plurality of enabling signals each changing from a non-active rest condition to an active normal condition and thereafter remaining at said active normal condition, said plurality of enable signals changing from the rest condition to the normal condition one at a time at predetermined time intervals following the initial switch one; and logic circuitry (20) for receiving the enable signals and sequentially enabling the producing of the sub-clocking signals.

8. A device according to claim 7, wherein the logic circuitry (20) comprises means (22_0-22_3) for ANDing respective enable signals with the master clock.

9. A device according to claim 8, wherein the logic circuitry (20) comprises a number of AND gates (22_0-22_3) corresponding to the number of enable signals, each AND gate (22_0-22_3) having a first input (24_0-24_3) for receiving its respective enable signal and a second input (26_0-26_3) for receiving the master clocking signal, said sub-clocking signals being produced at the respective outputs of said AND gates.

10. Digital processing apparatus comprising: a device in accordance with claim 2, and a plurality of discrete data processing parts, each of said data processing parts being clocked by a respective one of said plurality of sub-clocking signals.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE